CLAIMS

We claim:

1. A method for fabricating a Vss line in a memory device, comprising:
forming a plurality of memory cells above a semiconductor substrate;
forming a channel between two of said memory cells;
forming an oxide/nitride/oxide stack above said memory cells and said channel;
removing a portion of said oxide/nitride/oxide stack between said memory cells to expose said semiconductor substrate;
removing said oxide/nitride/oxide stack above the gates of said memory cells;
forming a plurality of source regions in said substrate between said memory cells;
forming a poly-silicon layer above said memory cells and said channel to connect to said source regions; and
removing a sufficient portion of said poly-silicon layer to form a Vss line.

2. The method as recited in Claim 1 wherein said memory cells are implemented as flash memory cells.

3. The method as recited in Claim 2 wherein said memory cells comprise:
a tunnel oxide above said semiconductor substrate;
a floating gate above said tunnel oxide;
an isolating region above said floating gate; and
a control gate above said isolating region, wherein said memory cell is programmed by storing a charge in said floating gate and current flow between said source and said drain is affected by said stored charge.

4. The method as recited in Claim 3 wherein said isolating region comprises:
a first oxide layer above said floating gate;
a nitride layer above said first oxide layer; and
a second oxide layer above said nitride layer.

5. The method as recited in Claim 4 wherein said oxide is an oxide of silicon.

6. The method as recited in Claim 4 wherein said nitride is a nitride of silicon.

7. The method as recited in Claim 1 wherein said channel is a Vss channel.

8. The method as recited in Claim 1 wherein said forming an oxide/nitride/oxide stack comprises:
forming a first oxide layer above said semiconductor substrate;
forming a nitride layer above said first oxide layer; and
forming a second oxide layer above said nitride layer.

9. The method as recited in Claim 8 wherein said oxide is an oxide of silicon.

10. The method as recited in Claim 9 wherein said nitride is a nitride of silicon.

11. A memory cell comprising:

a source;

a drain coupled to said source;

a Vss connection, coupled to said source;

a gate structure coupled to said source and said drain, said gate disposed so as to affect electrical flow between said source and said drain; and,

an isolating layer disposed so that said gate structure is enabled to retain a charge for an extended period of time.

12. The memory cell recited in Claim 11 wherein said extended period is a period in excess of one year.

13. The memory cell recited in Claim 11 further comprising a spacer disposed between said gate structure and said Vss connection.

14. The memory cell recited in Claim 13 wherein said spacer comprises an oxide/nitride/oxide stack.

15. The memory cell recited in Claim 14 wherein said oxide is an oxide of silicon.

16. The memory cell recited in Claim 14 wherein said nitride is a nitride of silicon.

17. A non-volatile memory device, comprising:

a plurality of non-volatile memory cells in an array;

a word line coupled to a row of said non-volatile memory cells;

a bit line coupled to a column of said non-volatile memory cells;

a plurality of drain regions coupled to said non-volatile memory cells;

a plurality of source regions coupled to said non-volatile memory cells; and

a Vss connection, coupled to a row of said source regions.

18. The non-volatile memory device as recited in Claim 17 wherein said memory device is formed on a silicon substrate.

19. The non-volatile memory device as recited in Claim 18 wherein source regions are formed in said silicon substrate by ion implantation.

20. The non-volatile memory device as recited in Claim 19 wherein said Vss connection is formed above said plurality of source regions.

21. The non-volatile memory device as recited in Claim 20 wherein said Vss connection is formed of poly silicon.

22. The non-volatile memory device as recited in Claim 17 wherein a cell in said plurality of non-volatile memory cells comprises;

a source;

a drain coupled to said source;

a Vss connection, coupled to said source;

a gate structure coupled to said source and said drain, said gate disposed so as to affect electrical flow between said source and said drain; and,

an isolating layer disposed so that a stored charge is enabled to affect the influence of said gate on said electrical flow between said source and said drain for an extended period.

23. The non-volatile memory device as recited in Claim 22 wherein said isolating layer comprises an oxide/nitride/oxide stack.

24. The non-volatile memory device as recited in Claim 23 wherein said isolation oxide/nitride/oxide stack comprises:

a first oxide layer above said semiconductor substrate;

a nitride layer above said first oxide layer; and

a second oxide layer above said nitride layer.

25. The non-volatile memory device as recited in Claim 24 wherein said oxide is an oxide of silicon.

26. The non-volatile memory device as recited in Claim 24 wherein said nitride is a nitride of silicon.